WHAT IS CLAIMED IS:

1. A computer system comprising:

a host processor;

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a switch for decoupling said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus, wherein the switch is an integrated part of the memory circuit.

2. The computer system of Claim 1 comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

3. The computer system of Claim 1, wherein the memory circuit comprises a synchronous DRAM memory.

4. A computer system comprising:

a host processor;

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a switch for decoupling said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus,

wherein the switch, the memory circuit and the memory controller are integrated into a single circuit.

5. The computer system of Claim 4, additionally comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

6. The computer system of Claim 4, wherein the memory circuit comprises a synchronous DRAM memory.

7. A computer system comprising:

a host processor;

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit;

a state decoder for receiving a chip select signal targeted for the memory circuit; and

a switch for decoupling said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus, and wherein the switch decouples said data base from said memory circuit in response to a change in state in the chip select signal.

8. The computer system of Claim 7, additionally comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

9. The computer system of Claim 7, wherein the memory circuit comprises a synchronous DRAM memory.

10. A computer system comprising:

a host processor;

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a switch for decoupling said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus,

wherein the switch, the memory circuit and the memory controller are integrated into a single circuit.

11. The computer system of Claim 10, comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

12. The computer system of Claim 10, wherein the memory circuit comprises a synchronous DRAM memory.

13. A computer system, comprising:

a host processor;

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

means for decoupling said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus.

14. The computer system of Claim 13 comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

15. The computer system of Claim 13, wherein the memory circuit comprises a synchronous DRAM memory.